FPGA Reconfigurable Convolution Accelerator

Design Survey and Proposal

David Cain,   
VLSI Lab  
University of Louisiana at LafayetteLafayette, Louisiana

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*Abstract*—A growing trend in modern computing and data processing is a deep learning algorithm application called Convolutional Neural Networks (CNNs). These processing algorithms rely on computationally intensive steps of matrix convolution that will restrict total system performance based on many factors. Software implementations are much too slow for modern data throughput requirements, as a result, Field Programable Gate Arrays (FPGAs) are often used for realizing CNNs on hardware. FPGAs allow for flexible design implementation while consistently improving energy efficiency levels with time. This paper reviews current implementations of FPGA based convolution accelerators with data throughput, data type flexibility, energy efficiency, and hardware utilization, under analysis. This paper also implements a prototype reconfigurable convolution accelerator design on Xilinx Pynq Z2 as the target device.

Keywords— Convolutional neural network, Matrix convolution, Reconfigurable FPGA, image recognition.

# Introduction

Convolutional Neural Networks are deep learning algorithms that are heavily based on matrix convolution, also simply named convolution. Convolution composes of more than 90% of the operations in a CNN application [1]. Therefore, peak data throughput capability of the convolution processing elements (PEs) within a CNN are fundamental for ensuring suitable performance of the total system. This matrix convolution is a multidimensional operation that occurs many times as a filter set is slid across an image to produce a feature map. The filter is often a 3x3, 4x4, or 5x5 array of pixel weights but will vary on application.

In

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*a**b* 

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